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NC7033
MNOS EAROM
21 x 16 (336 BIT)

GENERAL DESCRIPTION

The NC7033 is a low-cost 21 word by 16-bit electrically alterable nonvolatile memory designed especially for use in those systems which require secure, yet alterable, data storage. Data integrity is maintained for a minimum of one year between rewrites and is immune to sudden power outages.

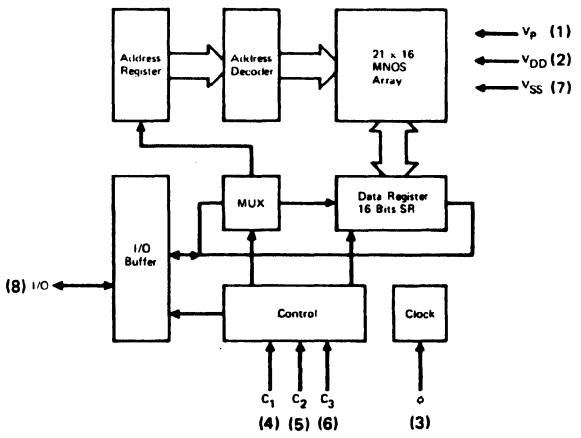
FEATURES

- 21 x 16 Organization
- Low-cost Packaging
- Serial Input/Output
- Fully Decoded Addressing
- Single-word Alterable
- Simple Interface Requirements
- Simple Refresh Capability
- Typical 10-year Unpowered Retention

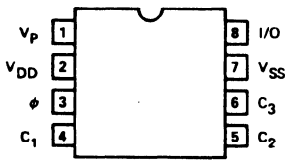
APPLICATIONS

- Microprocessor Peripheral Memory
- Backup Memories
- Preset Frequency Tuning for TVs
- Numerical Machine Controls
- Process Controllers
- Remote or Portable Data Acquisition Systems
- Storage of Calibration or Test Constants
- Programmable Locks/Security Systems
- Non-Volatile Counters, Odometers
- Programmable Games
- Appliance Timer/Controllers
- Event Monitors
- Automatic Telephone Dialers
- Traffic Lights
- Utility Meters

BLOCK DIAGRAM



PIN CONNECTION



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ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
Storage Temperature (Power Off) (NC7033L)	−55°C to +150°C
Storage Temperature (Power Off) (NC7033P)	−55°C to +125°C
Non-Powered Data Storage	−20°C to +100°C
Voltage, any Pin except V_P	V_{SS} +0.3V to V_{SS} −20V
Voltage at V_P, all others to V_{SS}	V_{SS} +0.3V to V_{SS} −38V

DC OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 10V ±1.0V, V_{DD} = 0V, V_P = −20V ±1.0V

SYMBOL	PARAMETER	PIN	UNITS	MIN	TYP	MAX	TEST CONDITIONS
I_{SS}	V_{SS} Supply Current	V_{SS}	mA			20	All Modes
I_P	V_P Supply Current	V_P	mA			8	All Modes
V_{OH}	Output High Voltage	I/O	V	V_{SS}−0.8			I_{OH} = 0.4mA, V_P = V_P, V_{DD}
V_{OL}	Output Low Voltage	I/O	V			V_{DD}+0.8	I_{OL} = 0.25mA, V_P = V_P
					V_{DD}+3.5		V_P = V_{DD}
I_{OHS}	Output Short Circuit Drive Capability	I/O	mA	6.0		12	V_{IH} = V_{DD}
I_{OLS}				−8.0		−20	V_{IL} = V_{SS}
	Pull-Ups to V_{SS}	C_1, C_2, C_3, ϕ	μA	15			V_{IH} = V_{SS} − 0.8V
						300	V_{IL} = V_{DD}
V_{IH}	Input High Voltage	I/O, C1, C2, C3, ϕ	V	V_{SS}−0.8		V_{SS}+0.3	
V_{IL}	Input Low Voltage			V_{DD}		V_{SS} −4.6	
	Pin Capacitance	I/O, C_1, C_2, C_3, ϕ	pF			10	Pin to V_{SS}
N_H	Data Retention (Power Off or Standby Modes)	–		1.0 yr.	3.0 yr.		≤10^5 E/W cycles
				2.5 yr.	10 yr.		≤ 10^2 E/W cycles

AC OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 10V ±1.0V, V_{DD} = 0V, V_P = −20V ±1.0V

SYMBOL	PARAMETER	PIN	UNITS	MIN	TYP	MAX	CONDITIONS
FCL	Clock Frequency FCL = 1/TCL	ϕ	kHz			100	
t_{CLH}	Clock High Level Hold Time	ϕ	μs	5		$10^{(1)}$	See Figure 1A
t_{CLL}	Clock Low Level Hold Time	ϕ	μs	5			
t_{CL}	Clock Fall Time and Rise Time	ϕ	μs			1	
t_{ERASE}	Erase Time	–	ms	150	300	450	See Figure 1E
t_{WRITE}	Write Time	–	ms	2.0	4.0	6.0	
t_E/t_W	Erase to Write Time Ratio	–		50	75	100	
t_{READ}	Read Access Time (First Bit)	I/O		1 clock cycle			
t_1 (2)	Data Out Delay	I/O		50ns		5.0 μs	See Figure 1A
t_2	Data In Setup	I/O	μs	2			See Figures 1A, 1B
t_3	Instruction Setup Lead	C_1, C_2, C_3	μs	2			See Figures 1B, 1C, 1D, 1E
t_4	Input Setup Lag		ns	50			
	V_P Slew Rate	V_P	V/μsec			1	Power On, Off
N_R	Number of Read Cycles	–		10^9	10^{10}		
N_E	number of Erase Cycles	–		10^5	10^6		
N_W	Number of Write Cycles	–		10^5	10^6		

NOTES: 1. Independent of clock frequency t_{CLH} maximum is 10μsec.
2. t_1 applies only during data transition.
3. Output external loading capacitance will be 10pF.

FUNCTIONAL DESCRIPTION

The NC7033 336-bit Metal-Nitride-Oxide Semiconductor (MNOS) array is organized into 21 rows of 16 bits. Each bit of storage is actually a dual-transistor pair, differentially sensed, one of which is charged to represent a logic "1" or "0". Each entire 16-bit row, or word, is individually addressable and alterable by means of three control lines (C_1, C_2 and C_3) and a serial input/output port. In addition, the NC7033 utilizes advanced MNOS technology by eliminating the need for programming voltage (V_P) for all but ERASE and WRITE operations.

Each operation is initiated by the proper sequencing of control lines followed by the appropriate 5-bit binary address code presented to the I/O port. The corresponding operation is then completed by the external clock. When not in use the NC7033 should be left OFF or in either a SETUP or STANDBY condition for maximum data retention. Pull up resistors and protection diodes are on C_1, C_2, C_3 and clock inputs. I/O pull up is active only during SERIAL ADDRESS IN and SERIAL DATA IN. During SERIAL DATA OUT, I/O operates in a push-pull mode. All other modes I/O is high impedance. The following mode control functions are provided:

TABLE 1

C_1(1)	C_2(1)	C_3(1)	Instruction	V_P Pin(2)
0	0	0	SETUP	V_P
0	0	1	ERASE	V_P
0	1	0	WRITE	V_P
0	1	1	SERIAL DATA OUT	V_P, V_{DD}(3)
1	0	0	SERIAL ADDRESS IN	V_P, V_{DD}, Hi Z
1	0	1	SERIAL DATA IN	V_P, V_{DD}, Hi Z
1	1	0	READ	V_P, V_{DD}
1	1	1	STANDBY	V_P, V_{DD}, Hi Z

NOTES: 1. $V_H = 1$, $V_L = 0$.
2. V_P can remain at its nominal voltage, or be switched to one of the conditions indicated.
3. Speed and output level will be degraded with V_P held at V_{DD}.

Read Mode

1. The (3-bit parallel) SERIAL ADDRESS IN instruction code is presented on C_1, C_2 and C_3 while the 5-bit serial address is shifted in on the I/O bus by five clocks. The 5-bit serial address utilizes a binary decoding scheme to address all 21 words. The most significant bit enters the chip first.
2. The READ instruction is presented for one clock time. This catches the word from the new address in the NVM array and parallel-loads it into a shift register. During READ the I/O port has an active tri-state output.
3. The SERIAL DATA OUT instruction is presented for 16 clock pulses, causing the data to be shifted out on the I/O bus. Data is handled on a first-in, first-out basis. If, after 16 bits of data has been read out the control lines are left in a SERIAL DATA OUT instruction code, the data will be circulated internally to allow further readout of the same data without access to the NVM array.

Erase/Write Mode

An ERASE must precede a WRITE for any location for data to be valid. However, a location can be pre-erased and left in an erased state anytime prior to the next write.

1. The address is changed, if necessary, in the same manner as in the read mode.
2. Data is serially loaded onto the chip by presenting the SERIAL DATA IN instruction for 16 clock pulses.
3. The SETUP instruction is presented for one clock pulse.
4. The ERASE instruction is presented for a nominal 300msec: this erases only the addressed word.
5. The SETUP instruction is presented again for one clock pulse.
6. The WRITE instruction is presented for nominal 4 milliseconds. This transfers the data to the selected address in the NVM.

If a location is written without an intervening erase cycle and with different data the result will be a random readout because both transistors in the bit-pair will be in a high state.

Erase Mode

In addition to the ERASE/WRITE sequence described above for an individual word address, all or part of the NC7033 can be pre-erased and left ready to initiate a WRITE sequence. Such would be the case if the NC7033 were to be used as a backup memory and data transferred in the event of a power failure.

1. The address is changed in the same manner as in the readout.
2. SETUP instruction is presented for one clock pulse.
3. ERASE instruction is presented for a nominal 300msec.
4. SETUP instruction presented again for one clock pulse.
5. Address is changed again as in #1 above and process repeated as often as desired.

It should be noted that because the ERASE mode brings both transistors in the bit-pair to a low state, it does not return the data to an all-logic "0" state but rather acts as a preconditioning to the array for the next WRITE pulse. If a READ is performed after a location has been erased but not rewritten the result will be a random pattern readout.

Standby

The STANDBY instruction puts the memory in a quiescent state where the output is high impedance and the clock is ignored.

Clock

The clock performs two functions; it enables mode changes and moves address and data information on the I/O line. A clock pulse is necessary only to enter or exit a mode and can be turned off during Erase, Write, Setup and Standby. Clock can stop during any of the remaining modes (SERIAL ADDRESS IN, SERIAL DATA IN, SERIAL DATA OUT) but data movement will be halted.

Setup

The SETUP instruction is necessary for the ERASE and WRITE modes. It isolates the particular addressed row and prevents adjoining rows or words from being inadvertently disturbed. The NC7033 can be left in SETUP without any loss of performance.

Retention

Data retention is a measurement of data validity between refresh (rewrite) cycles. The ability to alter data yet retain it during power interruptions is unique to MNOS-LSI. Both features of alterability and retention are interrelated and require clarification. The time in which data remains valid is inversely related to the number of rewrite/refresh cycles (see Figure 2). Excessive overstress of the nitride layer by too many erase and write cycles diminishes its ability to retain a charge.

Typically, long retention is not required for most applications. Data is normally altered or rewritten long before there is any danger of loss.

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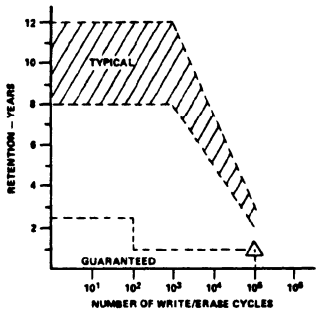

Figure 2. Retention Characteristics of MNOS.

INSTRUCTION SEQUENCES

With the exception of the ERASE mode, instructions may be presented in any random sequence without disturbance of data stored in the MNOS array. For the Erase mode the instruction sequence SETUP–ERASE must be followed.

Normal sequence of operation is as follows:

1. Power On (and Off) should be made in the absence of SETUP, ERASE or WRITE instruction codes. The power supplies then can be turned on or off in any sequence without disturbance of the data. Note that when V_P is open circuit or at V_{DD} the data in the array is always protected indpendent of the instruction being clocked in.
2. Select SERIAL ADDRESS IN command.
3. Chip is addressed for five clocks to enter five bits of address. The 5-bit binary address code (00000 to 10100) shifts the MSB into the chip first (see Figure 1B).
4. Other functions on the selected address can be performed as shown in Figures 1C, 1D and 1E.

SERIAL ADDRESS IN DECODING

WORD	MSB B5	B4	B3	B2	LSB B1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0

B5 ENTERS THE CHIP FIRST
B1 ENTERS THE CHIP LAST

TYPICAL INTERFACE SCHEMATICS